24.3 A 64b Adder Using Self-Calibrating Differential Output Prediction Logic

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A 64b adder, based on self-calibrating differential output prediction logic (OPL), was designed and fabricated using the 0.13µm IBM 8RF process. The adder had a normalized worst-case delay of 3.9 FO4 inverter delays. It is 1.8X faster, and used 2X lower energy compared to the best previously published 64b adder results, which were based on domino logic [1].

In OPL, each circuit path consists of a sequence of low-skew (precharge high) dynamic gates. For any critical path, at most every other gate has to make a transition [2]. Thus, OPL is shown to be twice as fast as domino logic for the same-size logic transistors since in the worst-case, every gate in a domino path would have to pull up. However, its main challenge is the generation and distribution of a plurality of clock phases with small separations and small skews. Nonetheless, several successful chips have been fabricated [3, 4]. Energy consumptions, however, were not improved over domino.

In this work, self-calibrating differential OPL (DOPL) is described. DOPL is slightly faster than OPL, but it offers lower energy consumption and inherently better reliability. DOPL is also inherently contention free (Fig. 24.3.1). When the clock is low, OUT and OUTB are precharged to V_{dd}, and thus keepers P3 and P1 are off. When the clock is high, one of the keepers is always off, and the other one is only fully turned on after OUTB finishes evaluation. By eliminating contention energy and by removing the large driver inverter used by domino gates, DOPL gates consume 38% lower power than conventional domino, for the same-size logic transistors.

An energy-efficient interleaved self-calibrating clock scheme is developed for DOPL in order to increase robustness with respect to PVT variations, for generating clock edges that are separated by less than an FO4 delay. A NAND2 gate is connected to the complementary outputs (OUT and OUTB) of a DOPL gate to generate a "done" signal that will be used for gates at a subsequent logic level. Since the computation of the "done" signals takes at least as long as a typical logic level in the very fast DOPL technique, the "done" signal is fed two levels forward as shown in Fig. 24.3.2. All the outputs of the NAND2 gates in each level are wired (meshed) together to generate a low-skew clock signal. Delay-matched clock trees generate the clocks for the first and second logic levels, where the second clock phase is delayed from the first phase by a transmission gate.

The "done" signal is generated by means of a precharged-low dynamic PMOS NAND2 gate. The use of dynamic gates reduces the loading on the DOPL gates, and more importantly, yields a much better clock edge since the hundreds or thousands of "done" signal gates whose outputs are connected in parallel produce no contention and therefore the "done" (or clock) edge rises monotonically. Given the large load on these parallel NAND2 gates, the clock edge (for two levels forward) does not begin to rise appreciably until a majority of dynamic NAND2s pull up. DOPL gates in a given logic level are therefore sized, taking into account their respective extracted loads, to have about the same delay.

The key concern with OPL circuits is the early arrival of a rising clock edge that can happen due to PVT variations if there is inadequate margin on the clock separations. The worst case occurs when an early-arriving clock edge causes the output of an OPL gate to start to fall when it should remain high, and then it will have to recover by means of the keeper (resulting in a "glitch"). The glitch will slow down subsequent gates receiving this input, and increases the possibility of even worse glitches downstream. The proposed self-calibrated DOPL technique suppresses output glitches. If a DOPL gate at the second logic level has a significant output glitch, then its "done" signal will be delayed, which then delays the issuance of the clock two levels forward (level 4) and thereby adds margin to that level. This provides more time for the third-level DOPL gate to fall and thus stops glitch propagation. In addition, the slower fall time of the third-level DOPL gate delays the fifth clock, further suppressing the original glitch. Note too that this scheme speeds up late-arriving clocks as well, since a late-arriving clock leads to a faster "done" signal, and thereby speeds up downstream clocks as appropriate.

The "done" signal logic is sized so that the worst-case glitch on any DOPL gate output never falls below 0.7-times V_{dd}. After sizing the whole adder, variational analysis is performed using 500 simulations on a full 3D extracted netlist, where each simulation involved the application of a random input vector and a random assignment of channel lengths (±20% of the nominal 0.12µm, using a normal distribution) for each adder transistor. The variational analysis showed that no output glitch ever falls below 0.5-times V_{dd}, and that is quite acceptable. Empirical analysis shows that the use of the "done" signal dynamic NAND2 gates for clock distribution reduces clock distribution energy by 13% compared to the static buffer clock-distribution scheme that is used by domino for the same clock loading. Thus, the self-calibrated DOPL logic technique consumes 50% less energy (38% less due to the improved keeper and 13% due to clock distribution).

The proposed 64b hybrid adder consists of a valency-3 Kogge-Stone sparse carry tree along with 3b carry-select modules. The components of the valency-3 Kogge-Stone sparse carry tree are represented by the equations in Fig. 24.3.3. The first 3 levels of the carry tree are implemented using DOPL gates in which only one of the two outputs (OUTB) is used. For the fourth level, both of the complementary output signals are used to select the correct sum from the 3b carry-select modules. To minimize energy consumption, relatively complex gates (Fig. 24.3.4) are used to implement the 3b carry-select module.

The worst-case delay over a set of 64b adder chips is measured to be nominally 238ps at 1.2V, with the fastest chip having a worst-case delay of 215ps. The measured FO4 inverter delay is 61ps at 1.2V, yielding a nominal normalized delay of 3.9 and a best case of 3.5. The adder consumes 30pJ. In a 90nm technology, we conservatively estimate the adder to consume 17.2pJ, nearly 2X lower than in [1], as presented in Fig. 24.3.5. Figure 24.3.6 shows the worst-case delay as the power supply is reduced to 0.7V.

References:

[1] R. Zlatanovici and B. Nikolic, "Power-Performance Optimal 64-bit Carry-Lookahead Adders," *Proc. ESSCIRC*, pp. 321 - 324, Sept., 2003.
[2] L. McMurchie, et al., "Output Prediction Logic: A High Performance CMOS Design Technique," *Proc. ICCD*, pp. 247-254, Sept., 2000.
[3] X. Guo and C. Sechen, "A High Throughput Divider Implementation," *Proc. IEEE CICC*, Paper 15.2, Sept., 2005.
[4] Y. Han, L. McMurchie and C. Sechen, "A High Performance CMOS Programmable Logic Core," *Proc. IEEE CICC*, pp. 449-452, Oct., 2004.

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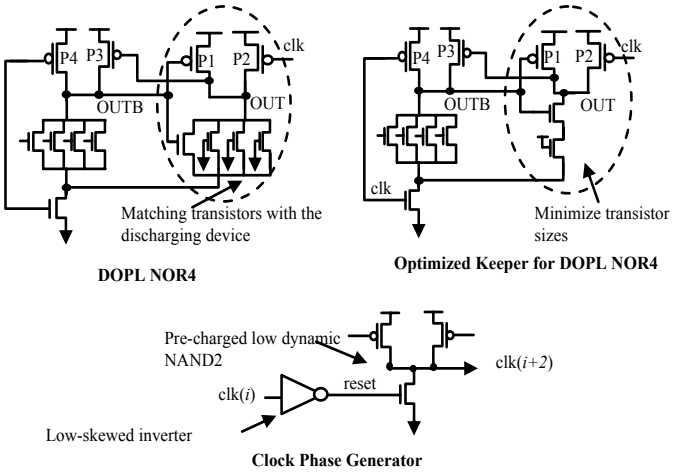


Figure 24.3.1: Schematic view of self-calibrating DOPL components.

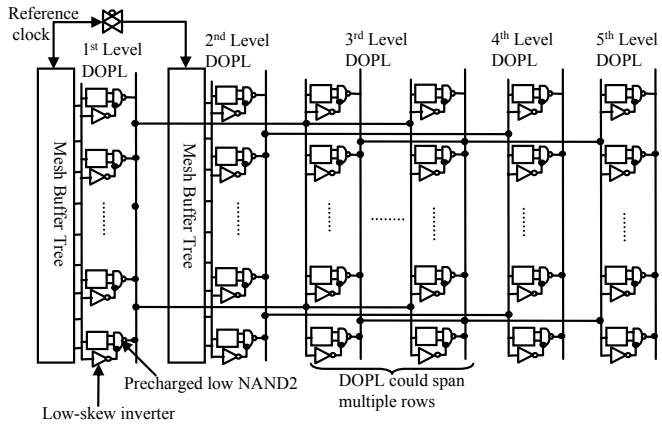


Figure 24.3.2: Self-calibrating DOPL floorplan.

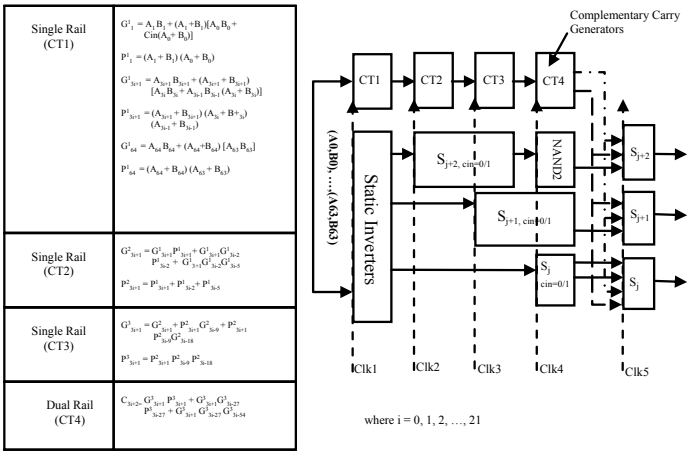


Figure 24.3.3: Valency-3 Kogge-Stone sparse carry tree and 3b carry-select block.

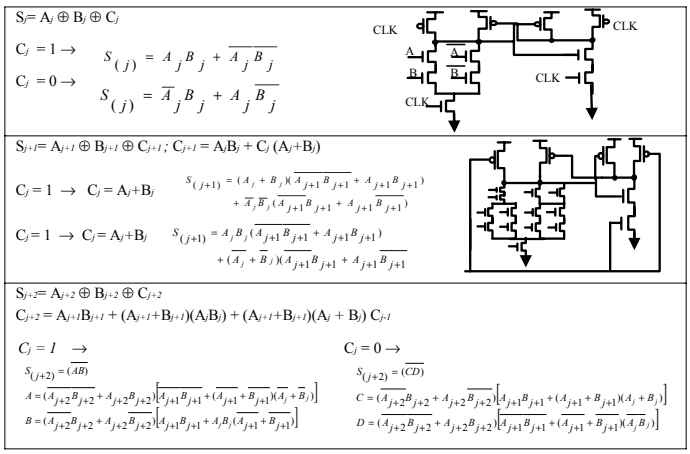
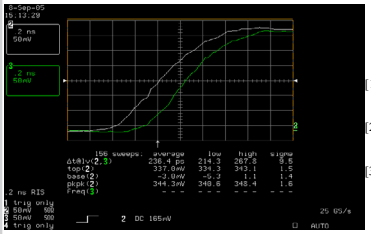


Figure 24.3.4: 3b carry-select equations and implementations.

Comparison of State-of-the-Art 64b Adders					
Delay/Energy / Logic Families	Adder Delay (FO4)	Actual Adder Energy (pJ)	Process	Estimated Adder Energy in 90nm (pJ)	References
Differential OPL including clock distribution tree	3.9 (1.0)	29.5	IBM 0.13µm 1.2V CMOS	17.17 (1.00)	
Domino logic including clock distribution tree	6.8 (1.8)	33.5	90nm 1.1V CMOS	33.5 (1.95)	[1]
Dynamic OPL including clock distribution tree	4.7 (1.2)	325	TSMC 0.18µm 1.8V CMOS	60.63 (3.53)	[2]
Static logic	11.7 (3.0)	54	ST 0.18µm 1.8V CMOS	10.07 (0.58)	[3]



$$Estimated\ Energy = Actual\ Energy \times \left(\frac{C_{process} \times Vdd^2}{C_{90\ nm} \times 1.1^2} \right)$$

[1] R. Zlatanovici and B. Nikolic, "Power-Performance Optimal 64- Bit Carry-Lookahead Adders," *Proc. ESSCIRC*, pp. 321-324, Sept., 2003.

[2] Shen Sun, Y. Han, X Guo, K.H. Chong, L McMurchie, C Sechen, "409ps 4.7 FO4 64b Adder Based on Output Prediction Logic in 0.18um CMOS," Proc. CSAS, pp. 52-58, May, 2005.

[3] S. Perri, P.. Corsonello, and G. Staino, "A Low Power Sub-Nanosecond Standard-Cells Based Adder," *Proc. IEEE ICECS* pp. 296-299, 2003.

Figure 24.3.5: 64b adder measured results.

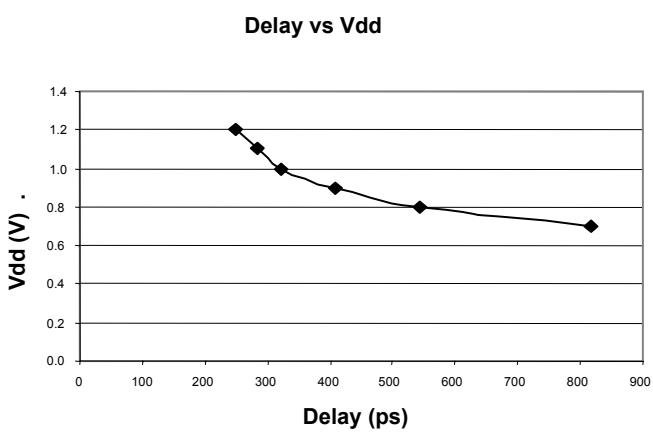


Figure 24.3.6: Delay versus Vdd curve for 64b DOPL adder.

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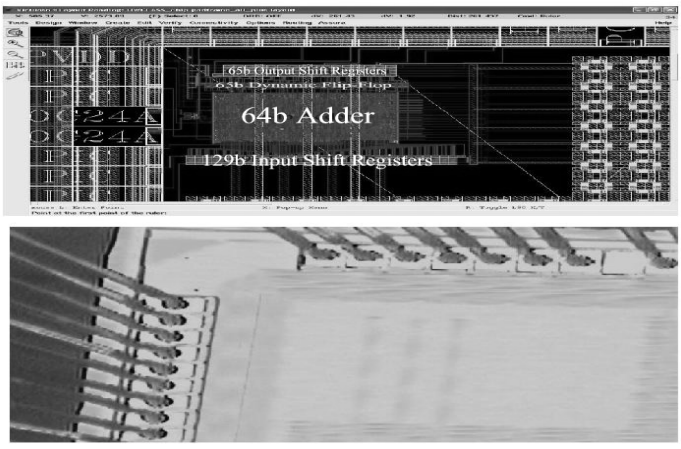

Figure 24.3.7: Adder layout and micrograph.

